ELEC 451 Introduction to Digital Integrated Circuits Syllabus

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Teaching Assistants:	No TA in this course
Class Hours:	Tuesday 9:30-12:30, room: Z13
Office Hour:	Tuesday 13:00-14:00
Textbook:	Weste & Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 3rd ed, Addison Wesley, 2005
Credits:	3(3+0+0) / 7.5 ECTS
Grading:	Homeworks: 40%
	Midterm : 20%
	Final Project : 40%

Catalog Description: The course covers fundamental theories and techniques of VLSI (Very Large Scale Integrated) design in CMOS (Complementary Metal-Oxide-Semiconductor) technology. The course starts with basic concepts and structures of designing VLSI systems including CMOS devices and circuits, standard CMOS fabrication processes, CMOS design rules, static and dynamic logic circuits, interconnect analysis, CMOS chip layout, simulation and testing, low power techniques, design tools and methodologies, and VLSI architecture. Also, students will gain design experience not only at schematic level but also at layout level.

Course learning objectives:

- Be able to use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnect.
- Be able to create models of moderately sized CMOS circuits that realize specified digital functions.
- Be able to apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect.
- Have an understanding of the characteristics of CMOS circuit construction and the comparison between different state-of-the-art CMOS technologies and processes.
- Be able to complete a significant VLSI design project having a set of objective criteria and design constraints.

Contribution to Program Learning Objectives:
The course contributes to the following program learning outcomes:

`Outcome-1` Knowledge of Mathematics, Science and Basic Electronics Engineering.

`Outcome-4.` Ability to design, develop, implement and maintain a complex system, process or product within realistic constraints and to meet defined requirements.

`Outcome-5.` Ability to identify, formulate and solve complex engineering problems encountered in engineering applications.

`Outcome-6.` Ability to identify different technical and modern tools in solving complex problems encountered in engineering applications and to develop the knowledge of following and using constantly updated information technologies.

`Outcome-11.` Ability to use modern methods and technical tools.

Course Outline:

1. Week: Introduction to VLSI technology
2. Week: A brief history of ICs, Design flow, Design Partitioning, Fabrication, Packaging, andTesting
3. Week: MOS Capacitor, I-V Characteristics, Gate and Diffusion Capacitance, Non-idealitiesand PVT
4. Week: Interconnect Modeling, Wire Resistance, Wire Capacitance, Wire RC Delay,Crosstalk, Wire Engineering, Repeaters

5. Week: Pass Transistors, DC Response, Logic Levels, Noise Margins, Transient Response,RC Delay Models, Delay Estimation, Logical Effort, Delay in a Logic Gate,Multistage Logic Networks, Choosing the Best Number of Stages
6. Week: Pseudo-nMOS Logic, Dynamic Logic, Pass Transistor Logic
7. Week: Transistor level combinational and sequential circuit design
8. Week: Midterm Exam
9. Week: Power and Energy: Dynamic Power and Static Power
10. Week: Scaling, Interconnect, Future Challenges, Testing, Fault Models ,Observability andControllability, Design for Test, Boundary Scan
11. Week: Variation, Noise Budgets, Reliability, Circuit Pitfalls
12. Week: Single-bit Addition, Carry-Ripple Adder, Carry-Skip Adder, Carry-Lookahead Adder Carry-Select Adder, Carry-Increment Adder, Tree Adder and Datapath
13. Week: Memory Arrays, SRAM Architecture, Serial Access Memories, Content-Addressable Memories, Read-Only Memories, Programmable Logic Arrays
14. Week: Packaging, Power Distribution, Clock Distribution Clock System Architecture, Phase-Locked Loops , Delay-Locked Loops
15. Week: Project Presentations
16. Week: Final Exam

Course Structure: The class meets for one lecture a week consisting of three 50-minute sessions.

Computer/Laboratory Resources: Google SkyWater SKY130 PDK will be used as technology models while **NGSPICE**, **XSCHEM**, and **MAGIC** are used for simulation, schematic, and layout, respectively.

♣ ♣ ♣ According to the Ethics Code of the Department, you have to perform all graded work individually. Copying the homework solutions from any source, be it another student, an assignment from a preceding term, etc., defeats the educational intent of the effort, and will be subject to disciplinary action. ♣ ♣ ♣